THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:

1. A method of packaging a high-density integrated circuit with at least one microchip disposed on a substrate comprising:
   (a) providing pre-insulated bond wires;
   (b) forming an array of coated bonding pads on said microchip; and
   (c) attaching said pre-insulated bond wires directly onto said bonding pads and directly onto terminal pads disposed on said substrate.

2. The method of packaging a high density integrated circuit according to claim **1**, wherein said bonding pads are located at selected locations on said microchip.

3. The method of packaging a high density integrated circuit according to claim **2**, wherein said bonding pads comprise a metallized aluminium, gold, or copper material.

4. The method of packaging a high density integrated circuit according to claim **1**, wherein said pre-insulated bond wires are selected from a group consisting of gold, aluminum, copper and combinations thereof.

5. The method of packaging a high density integrated circuit according to claim **1**, wherein said pre-insulated bond wires are attached onto said bonding pads by a ball shaped joint.

6. The method of packaging a high density integrated circuit according to claim **1**, wherein a plurality of microchips are disposed on said substrate and said bonding pads are located on the microchips.

7. The method of packaging a high density integrated circuit according to claim **6**, including attaching said pre-insulated bond wires to said bonding pads to thereby connect adjacent microchips.

8. A method of packaging a high density integrated circuit having at least one semiconductor microchip disposed on a substrate having a plurality of terminal pads provided thereon, comprising;
   (a) providing pre-insulated bond wires;
   (b) forming a plurality of bonding pads in a plurality of rows and columns over a surface of said microchip; and
   (c) connecting selected bonding pads on said microchip with selected terminal pads on said substrate with said pre-insulated bond wires.

9. The method of packaging a high density integrated circuit according to claim **8**, including coating the integrated circuit with a protective encapsulating material.

10. The method of packaging a high density integrated circuit according to claim **8**, wherein said bonding pads are located at selected locations over the entire surface of said microchip.

11. The method of packaging a high density integrated circuit according to claim **8**, wherein a plurality of semiconductor microchips are disposed on said substrate, and interconnections among selected bonding pads on said microchips are provided by pre-insulated bond wires bonded to said selected bonding pads.

12. The method of packaging a high density integrated circuit according to claim **11**, wherein said pre-insulated bond wires are selected from a group consisting of gold, aluminium, copper and combinations thereof.

13. An integrated circuit package comprising:
    (a) a substrate having terminal pads arranged in at least one row along a perimeter of a surface of said substrate;
    (b) vias connecting said terminal pads directly to connectors on an opposite side of said substrate;
    (c) a semiconductor chip mounted on the substrate, inside said perimeter, said chip having bond pads located on a surface of said chip; and
    (d) a plurality of insulated bond wires, each of said bond wires extending from a bond pad on said chip to a terminal pad on said substrate, said substrate being sized and shaped to provide a sufficient number of rows of terminal pads and associated vias so that horizontal traces through said substrate are not required.

14. An integrated circuit package as claimed in claim **13**, wherein said substrate is configured to contain a minimal number of layers, to reduce interlayer inductance, capacitance, and cross talk, and to increase the range of bandwidth performance.

15. An integrated circuit package as claimed in claim **14**, wherein said substrate is a single layer substrate.

16. An integrated circuit package as claimed in claim **14**, wherein said substrate contains no lead frames.

17. An integrated circuit package as claimed in claim **16**, wherein said opposite side of said substrate contains a ball grid array, and each of said terminal pads connects to a ball in said ball grid array through said via directly traversing said substrate.

18. An integrated circuit package as claimed in claim **13**, wherein said insulated bond wires extending between said bond pads on said chip and said terminal pads on said substrate are positioned to reduce parallelism between adjacent wires, to in turn reduce cross talk and increase the range of bandwidth performance.

19. An integrated circuit package as claimed in claim **18**, wherein said insulated bond wires are attached in a generally X or Y shaped pattern.

20. An integrated circuit package as claimed in claim **19**, wherein said generally X or Y shaped pattern is an in line or staggered X-Y grid pattern.

21. An integrated circuit package as claimed in claim **13**, wherein at least one of said bond pads is located in an interior portion of said surface of said chip.

22. An integrated circuit package as claimed in claim **21**, wherein said bond pad located in said interior portion is electrically connected to one of a power connection and a ground connection on said chip.

23. A method of manufacturing an integrated circuit package, said method comprising:

(a) providing a semiconductor chip having bond pads located on a surface of said chip, at least a portion of said bond pads being designated to provide input/output functions;

(b) providing a substrate having terminal pads arranged in at least one row along a perimeter of a surface of said substrate, said substrate having vias connecting said terminal pads directly to connectors on an opposite side of said substrate, said substrate being sized and shaped to contain

a sufficient number of rows of terminal pads and associated vias so that horizontal traces through said substrate are not required;

(c) mounting said semiconductor chip on said surface of said substrate, inside said perimeter; and

(d) connecting insulated bond wires between said portion of said bond pads and said terminal pads.

24. A method of manufacturing as claimed in claim **23**, wherein said step of connecting insulated bond wires in step (d) comprises positioning said bond wires to reduce parallelism between adjacent wires, to in turn reduce cross talk and increase the range of bandwidth performance.

25. A method of manufacturing as claimed in claim **23**, wherein said connectors on said opposite side of said substrate are balls in a ball grid array.